REMARKS

Upon entry of the reply into the record, claims 1-5, 7-17, 19-24 and 26-30 are pending. Of those, claims 1, 14 and 20 are independent.

By this reply, claims 6 and 25 have been canceled without prejudice to, or disclaimer of, the subject matter contained therein. Also by this reply, claims 27-30 have been added. Previously, claim 18 was canceled.

§103 Rejection: Only '519 Patent & Olukotun Ref. Combined

Beginning on page 3 of the Office Action, claims 1-4, 6, 12-15, 20-21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,532,519 to Arimilli (the '519 patent) in view of the publication authored by Olukotun et al. (the Olukotun reference). Applicant traverses.

At the top of page 7 of the Office Action, the Examiner asserts that the '519 patent teaches mapping a plurality of main memory address ranges to a plurality of caches. Again, Applicant traverses.

In support of the assertion, the Examiner directs Applicant's attention to the following passages, which are reprinted for convenience.

Lines 30-34 of Column 1

> [T]ertiary or L3 caches, may also be included in each processing unit for supporting the secondary caches. Each level of caches stores a subset of data and instructions contained in a system memory for low-latency accesses by various processor cores.

Lines 51-67 of Column 3

> Under the present invention, it is also possible for two or more L3 caches to be merged together, using an interleaving or other address partitioning policy, such that the merged L3 caches act as a single larger cache. With such merging, each L3 cache controller that participates in such a merged cache group has its mode register set to the same value such that all L3 cache controllers in the merged cache group act on behalf of the same subset of processing units. In such a case, the system initialization rule stated above is generalized such that each processing unit should end up with its corresponding

> processing unit field set to a logical "1" in the mode register of the L3 cache controller of one and only one cache group. Note that a cache group could be a single L3 cache controller or any number of merged L3 cache controllers, and there could be a mixture of cache group sizes in a given multi-processor data processing system.

Inspection of the above-quoted passages reveals that neither mentions a range of main memory addresses, much less a plurality of such ranges, much less mapping of such main memory address ranges to a plurality of caches. Applicant submits that the same is true (namely, no such mention) for the remaining portion of the '519 patent. Nor is such mapping disclosed by the Olukotun reference.

A distinction of independent claim 1 over each of the '519 patent and the Olukotun reference, as well as the combination thereof, is the plurality of caches being mapped to a plurality of main memory address ranges, respectively. Claims 2-4 and 12-13 depend at least indirectly from claim 1 and include at least this distinction by dependency.

Independent claim 14 recites a feature similar to the distinction of claim 1 noted above, which similarly is a distinction over the combination of the '519 patent and the Olukotun reference. Claim 15 depends from claim 14 and exhibits at least the distinction of claim 14 by dependency.

Claim 20 recites a feature similar to the distinction of claim 1 noted above, which similarly is a distinction over the combination of the '519 patent and the Olukotun reference. Claims 20, 23-24 and 26 depend from claim 20, respectively, and exhibit at least the distinction of claim 20 by dependency.

By this reply, claim 6 has been canceled. This makes the rejection of claim 6 moot.

By this reply, claim 25 has been canceled, making its rejection moot.

In view of the foregoing discussion, the § 103(a) rejection of claims 1-4, 6, 12-15, 20-21 and 23-26 over the combination of the '519 patent and

the Olukotun reference is improper and Applicant requests that it be withdrawn.

Other §103 Rejections

Beginning on pages 8 and 11, respectively, rejections of the remaining claims are made based upon the combination of the '519 patent and the Olukotun reference as modified by each of two tertiary references. More particularly, claims 5, 7-10, 16-17 and 18 are rejected (using as the tertiary reference U.S. Patent No. 5,737,757 to Hassoun et al.) beginning on page 8 while claims 11 and 19 are rejected (using as the tertiary reference the Handy reference) beginning on page 11. Applicant traverses.

Neither of the respective tertiary references discloses the distinctions over the combination of the '519 patent and the Olukotun reference, noted above.

Claims 5, 7-8, 10-11, 16-17, 19 and 22 depend at least indirectly from claims 1, 14 and 20, respectively, and thus exhibit at least the distinctions over the combination of the '519 patent Olukotun reference noted above, respectively. Accordingly, these distinctions thus represent distinctions over the combination of the '519 patent and the Olukotun reference with the respective third references.

In view of the foregoing discussion, the § 103(a) rejections of claims 5, 7-8, 10-11, 16-17, 19 and 22 are improper and Applicant requests that they be withdrawn.

New Claims 27-30

Again, claims 27-30 have been added. Claims 27-30 depend from claims 14 and 20, respectively, and exhibit at least their respective distinctions by dependency.

CONCLUSION

The issues in the case are considered to be resolved. Accordingly, Applicant again requests a Notice of Allowability.

Person to Contact

In the event that any matters remain at issue in the application, the Examiners are invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-2025 for any additional fees under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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